



SLUU232 -February 2006

Using the TPS40190EVM-001

A 12V Input, 1.5V Output, 10A Synchronous Buck Converter

System Power Management – DC/DC Controllers

1 INTRODUCTION

The TPS40190EVM-001 evaluation module (EVM) is a synchronous buck converter providing a fixed 1.5V output at up to 10A from a 12V input bus. The EVM is designed to start up from a single supply, so no additional bias voltage is required for start-up. The module uses the TPS40190 Reduced Pin Count Synchronous Buck Controller.

1.1 DESCRIPTION

TPS40190EVM-001 is designed to use a regulated 12V (10V-14V) bus to produce a high current, regulated 1.5V output at up to 10A of load current. The TPS40190EVM-001 is design to demonstrate the TPS40190 in a typical regulated bus to low-voltage application while providing a number of test points to evaluate the performance of the TPS40190 in a given application. The EVM can be modified to support output voltages from 0.9V to 3.3V by changing a single set resistor.

1.2 APPLICATIONS

- Non-Isolated Medium Current Point of Load and low voltage bus converters.
- Networking Equipment
- Telecommunications Equipment
- DC Power Distributed Systems

1.3 FEATURES

- 10V 14V input range
- 1.5V fixed output, adjustable with single resistor
- 10Adc Steady State Output Current
- 300kHz switching frequency (Fixed by TPS40190)
- Single Main Switch N-channel MOSFET and Single Synchronous Rectifier N-channel MOSFET
- Double Sided 3" x 3" PCB with all components on top side
- Active Converter uses less than 1.2 square inches 1.775 x 0.670
- Convenient test points for probing critical waveforms and non-invasive loop response testing

2 TPS40190EVM-001 ELECTRICAL PERFORMANCE SPECIFICATIONS

Parameter	Notes and Conditions		Min	Тур	Max	Units
INPUT CHARACTERISTI	CS					
Input Voltage Range			10		14	V
Max Input Current	$V_{IN} = 10V, I_{OUT} = 10A$			2		Α
No-Load Input Current	$V_{IN} = 14V$, $I_{OUT} = 0A$			100		mA
OUTPUT CHARACTERIS						
Output Voltage	R6 = 6.49k R5 = 10k		1.45	1.50	1.55	V
Output Voltage	Line Regulation (10V <v<sub>IN<14V, I_{OUT} = 5A)</v<sub>				1	%
Regulation	Load Regulation (0A <i<sub>OUT<10A, V_{IN} = 12V)</i<sub>				1	%
Output Voltage Ripple	$V_{IN} = 14V, I_{OUT} = 10A$			25	50	mVpp
Output Load Current			0		10	Α
Output Over Current				23		Α
SYSTEM CHARACTERIS	TICS					
Switching Frequency			240	300	360	kHz
Peak Efficiency	$V_{OUT} = 1.5V, 8A < I_{OUT} < 12A$	$V_{12V_{-}IN} = 10V$		87		
		$V_{12V_{-}IN} = 12V$		85		%
		$V_{12V IN} = 14V$		83		
Full Load Efficiency	$V_{OUT} = 1.5V, I_{OUT} = 15A$	$V_{12V_{-}IN} = 10V$		84		
		$V_{12V_{-}IN} = 12V$		83		%
		$V_{12V_{-}IN} = 14V$		81		

Table 1: TPS40190EVM-001 Electrical & Performance Specifications

3 SCHEMATIC

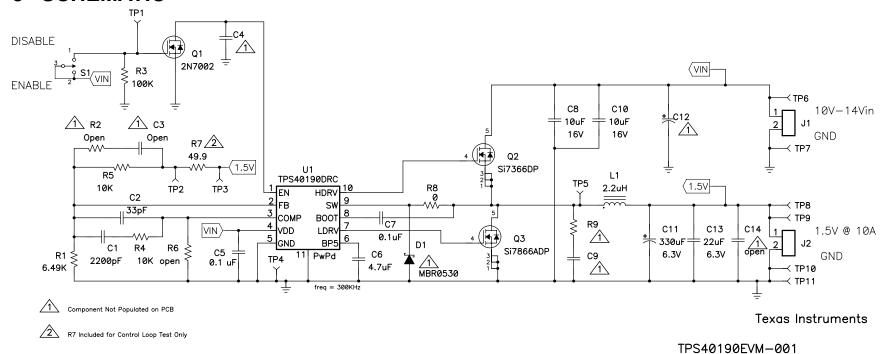


Figure 1: TPS40190EVM-001 Power Stage / Control Schematic

For Reference Only, See Table 3: Bill of Materials for Specific Values

3.1 ADJUSTING OUTPUT VOLTAGE (R1)

The regulated output voltage can be adjusted within a limited range by changing the ground resistor in the feedback resistor divider (R1). The output voltage is given by the formula

$$V_{VOUT} = V_{VREF} \times \frac{R5+R1}{R1}$$

Where $V_{VREF} = 0.591V$ and $R5 = 10K\Omega$

Table 2 contains common values for R1 to generate popular output voltages. TPS40190EVM-001 is stable through these output voltages but the efficiency may suffer as the power stage is optimized for the 1.5V output.

V_{OUT}	R1	
3.3V ¹	2.15K	
2.5V ¹	3.09K	
2.25V	3.57K	
2.0V	4.22K	
1.8V	4.87K	
1.5V	6.49K	
1.2V	9.76K	

Table 2: Adjusting Vout with R1

3.2 ADJUSTING SHORT CIRCUIT PROTECTION (R6)

The TPS40190 uses a selectable current limit for short circuit protection. The current limit is selected from 3 levels by placing a resistor at R6. The TPS40190 compares the voltage drop across the high-side FET (VDD to SW) to an internal reference voltage selected during start-up. The voltage levels are shown in Table 3.

V_{SCP}	R6	
160mV	3.9 K	
320mV	OPEN	
420mV	12 K	

Table 3: Adjusting V_{SCP} with R6

The current before declaring short circuit protection can be determined by dividing the V_{SCP} by the $R_{DS(ON)}$ of the High-Side FET (Q2)

3.3 DISABLE (TP1 & SW1)

TPS40190EVM-001 provides both a Disable input (TP1) and a Disable switch (SW1) to allow the user to evaluate the TPS40190's Enable Function. When the switch is ON or TP1 is pulled high, Q1 pulls EN (U1 Pin 1) to ground and disables the TPS40190 IC.

 $^{^1}$ For Output Voltages greater than 2.5V, Change C11 to $330\mu\text{F}$ 4V or higher PosCAP

TEST SET UP

3.4 EQUIPMENT

3.4.1 VOLTAGE SOURCE

V12V IN

The input voltage source (V_{12V_IN}) should be a 0-15V variable DC source capable of 5Adc. Connect V_{12V_IN} to J1 as shown in Figure 3.

3.4.2 METERS

A1: 0-5Adc, ammeter

V1: V_{12V_IN}, 0-15V voltmeter

V2: V_{1V5 OUT} 0-5V voltmeter

3.4.3 LOADS

LOAD1

The Output Load (LOAD1) should be an Electronic Constant Current Mode Load capable of 0-15Adc @ 1.5V

3.4.4 OSCILLOSCOPE

OSCILLOSCOPE

A Digital or Analog Oscilloscope can be used to measure the ripple voltage on V_{OUT} . The Oscilloscope should be set for $1\text{M}\Omega$ impedance, 20MHz Bandwidth, AC coupling, $1\mu\text{s}/\text{division}$ horizontal resolution, 20mV/division vertical resolution for taking output ripple measurements. TP 9 and TP 10 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP 9 and holding the ground barrel to TP 10 as shown in Figure 3. For a hands free approach, the loop in TP 10 can be cut and opened to cradle the probe barrel. Using a leaded ground connection may induce additional noise due to the large ground loop area.

3.4.5 Recommended Wire Gauge

 V_{13V} in to J1

The connection between the source voltage, V_{12V_IN} and J1 of the TPS40190EVM-001 can carry as much as 3 Adc. The minimum recommended wire size is AWG #16 with the total length of wire less than 4 feet (2 feet input, 2 feet return).

J2 to LOAD1 (Power)

The power connection between J2 of TPS40190EVM-001 and LOAD1 can carry as much as 15Adc. The minimum recommended wire size is 2x AWG #16, with the total length of wire less than 4 feet (2 feet output, 2 feet return).

3.4.6 OTHER

FAN

This evaluation module includes components that can get hot to the touch, because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200-400 lfm is required to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered. The EVM should not be probed while the fan is not running.

3.5 EQUIPMENT SETUP

Shown in Figure 3 is the basic test set up recommended to evaluate the TPS40190EVM-001. Please note that although the return for J1 and J2 are the same, the connections should remain separate as shown in Figure 2.

3.5.1 Procedure

- 1. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
- 2. Prior to connecting the DC input source, V_{12V_IN}, it is advisable to limit the source current from V_{12V_IN} to 5.0A maximum. Make sure V_{12V_IN} is initially set to 0V and connected as shown in Figure 2.
- 3. Connect the ammeter A1 (0-5A range) between V_{12V_IN} and J1as shown in Figure 2.
- 4. Connect voltmeter V1 to TP6 and TP7 as shown in Figure 2.
- 5. Connect LOAD1 to J2 as shown in Figure 2. Set LOAD1 to constant current mode to sink 0Adc before V_{12V IN} is applied.
- 6. Connect voltmeter, V2 across TP8 and TP11 as shown in Figure 2.
- 7. Connect Oscilloscope probe to TP9 and TP10 as shown in Figure 3.
- 8. Place Fan as shown in Figure 2 and turn on, making sure air is flowing across the EVM.

3.5.2 Diagram

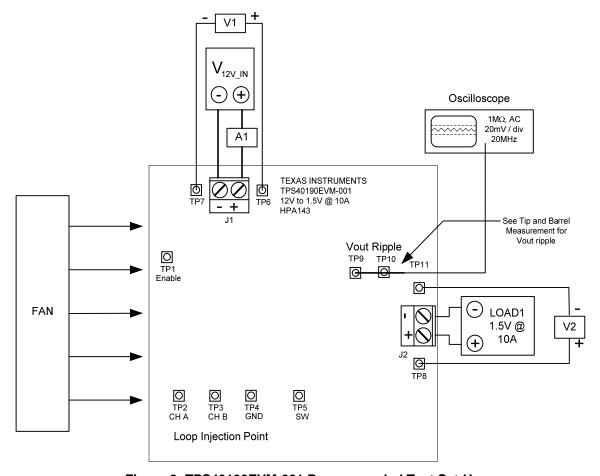


Figure 2: TPS40190EVM-001 Recommended Test Set-Up

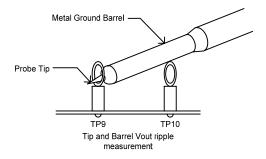


Figure 3: Output Ripple Measurement - Tip & Barrel using TP9 and TP10

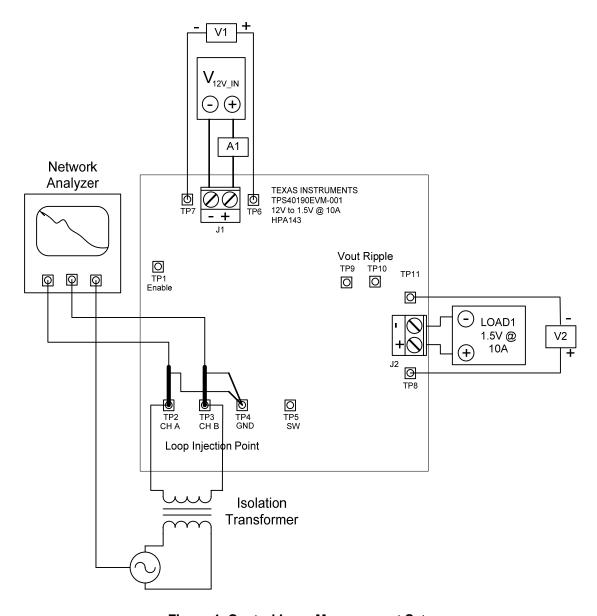


Figure 4: Control Loop Measurement Setup

3.6 START UP / SHUT DOWN PROCEDURE

- 1. Increase $V_{12V IN}$ from 0V to 10Vdc.
- 2. Vary LOAD1 from 0 10Adc
- 3. Vary V_{12V_IN} from 10Vdc to 14Vdc
- 4. Decrease LOAD1 to 0A.

3.7 CONTROL LOOP GAIN & PHASE MEASUREMENT PROCEDURE

- 1. Connect 1kHz 1MHz Isolation Transformer to TP2 and TP3 as show in Figure 4
- 2. Connect Input Signal Amplitude Measurement Probe (Channel A) to TP2 as shown in Figure 4
- 3. Connect Output Signal Amplitude Measurement Probe (Channel B) to TP3 as shown in Figure 4
- 4. Connect Ground Lead of Channel A and Channel B to TP 4 as shown in Figure 4
- 5. Inject 25mV or less signal across R7 through Isolation Transformer
- 6. Sweep Frequency from 1kHz to 1MHz with 10Hz or lower post filter
- 7. Control Loop Gain can be measured by $20 \times LOG \left(\frac{ChannelB}{ChannelA} \right)$
- 8. Control Loop Phase is measured by the Phase difference between Channel A and Channel B
- 9. Disconnect Isolation Transformer from TP2 and TP3 before making other measurements (Signal Injection into Feedback may interfere with accuracy of other measurements)

3.8 EQUIPMENT SHUTDOWN

- 1. Shut Down Oscilloscope
- 2. Shut down LOAD1
- 3. Shut down V_{12V_IN}
- 4. Shut down FAN

4 TPS40190EVM TYPICAL PERFORMANCE DATA & CHARACTERISTIC CURVES

Figure 5 & Figure 6 present typical performance curves for the TPS40190EVM-001. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

4.1 EFFICIENCY

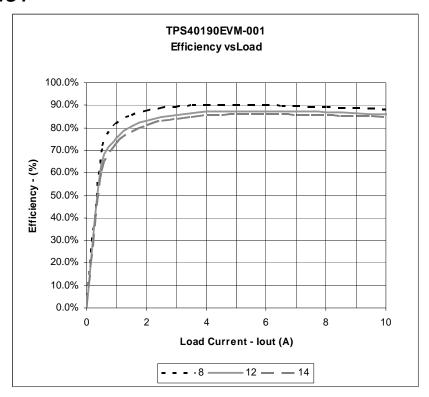


Figure 5: TPS40190EVM-001 Efficiency $V_{IN} = 10-14V$, $V_{OUT} = 1.5V$ $I_{OUT} = 0-10A$

4.2 LINE & LOAD REGULATION

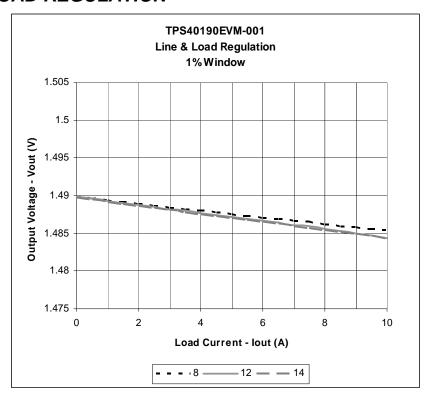


Figure 6: TPS40190EVM-001 Line & Load Regulation

5 EVM ASSEMBLY DRAWINGS AND LAYOUT

The following figures (Figure 7 through 12) show the design of the TPS40190EVM-001 printed circuit board. The EVM has been designed using a Double Sided, 2oz copper-clad circuit board 3.0" x 3.0" with all components on the top side to allow the user to easily view, probe and evaluate the TPS40190 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

Figure 7: TPS40190EVM-001 Component Placement (Viewed from Top)

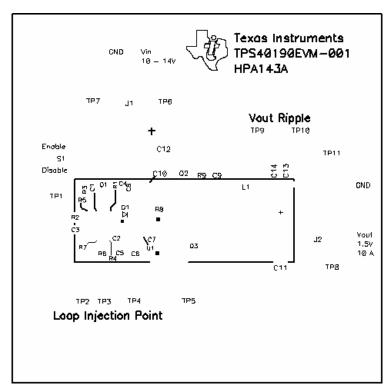


Figure 8: TPS40190EVM-001 Silkscreen (Viewed from Top)

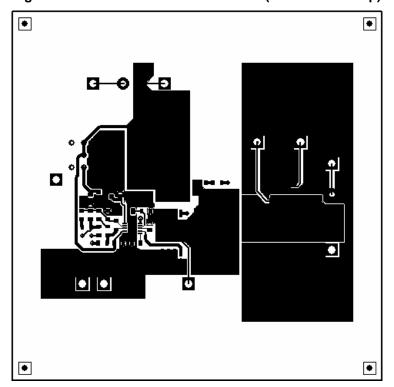


Figure 9: TPS40190EVM-001 Top Copper (Viewed from Top)

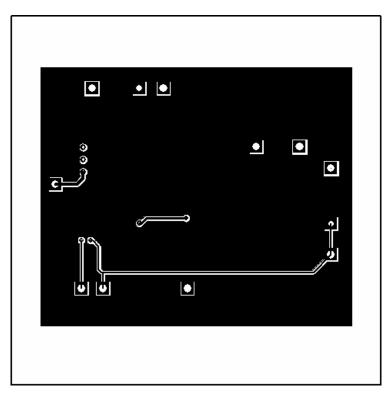


Figure 10: TPS40190EVM-001 Bottom Copper (X-Ray View from Top)

6 LIST OF MATERIALS

Table 3 lists the EVM components as configured according to the schematic shown in Figure 1.

Count	RefDes	Description	Size	Mfr	Part Number
1	C1	Capacitor, Ceramic, 2200pF, 50V, X7R	0603	Std	Std
1	C11	Capacitor, PosCAP, 330uF, 6.3V, 20%	7343	Sanyo	6TPB330M
0	C12	Capacitor, Aluminum, open	8x10mm		
1	C13	Capacitor, Ceramic, 22uF, 6.3V, X5R	1206	TDK	C3216X5R0J226KT
0	C14	Capacitor, Ceramic, open	1206		
1	C2	Capacitor, Ceramic, 33pF, 50V, C0G	0603	Std	Std
0	C3, C4, C9	Capacitor, Ceramic, open	0603		
2	C5, C7	Capacitor, Ceramic, 0.1uF, 16V, X5R	0603	Std	Std
1	C6	Capacitor, Ceramic, 4.7uF, 6.3V, X5R	0603	TDK	C1608X5R0J475KT
2	C8, C10	Capacitor, Ceramic, 10uF, 16V, X5R	1206	TDK	C3216X5R1C106KT
0	D1	Diode, Schottky, 0.5-A, 30-V	SOD123	On Semi	MBR0530T1
1	J1	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25	OST	ED1514
1	J2	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35	OST	ED1609
1	L1	Inductor, SMT, 2.2uH, 12.5A, 4 milliohm	0.492 sq"	Coiltronics	DR127-2R2
1	Q1	MOSFET, N-ch, 60-V, 115-mA, 1.2-Ohms	SOT23	Vishay	2N7002
1	Q2	MOSFET, NChannel, 20V, 16A, 9 millohm	PWRPAK S0-8	Vishay	Si7366DP
1	Q3	MOSFET, NChannel, 20V, 40A, 3.0 millohm	PWRPAK S0-8	Vishay	Si7866ADP
1	R1	Resistor, Chip, 6.49K-Ohms, 1/16-W, 1%	0603	Std	Std
0	R2, R6, R9	Resistor, Chip, Open, 1/16-W, 1%	0603	Std	Std
1	R3	Resistor, Chip, 100K Ohms, 1/16-W, 1%	0603	Std	Std
2	R4, R5	Resistor, Chip, 10K Ohms, 1/16-W, 1%	0603	Std	Std
1	R7	Resistor, Chip, 49.9 Ohms, 1/16-W, 1%	0603	Std	Std
1	R8	Resistor, Chip, Zero Ohms, 1/16-W, 1%	0603	Std	Std
1	S1	Switch, ON-ON Mini Toggle	0.28 x 0.18		633-G12AP
4	TP1, TP2, TP3, TP5	Test Point, White, Thru Hole	0.125 x 0.125	Farnell	5012
4	TP4, TP7, TP10, TP11	Test Point, Black, Thru Hole	0.125 x 0.125	Farnell	5011
3	TP6, TP8, TP9	Test Point, Red, Thru Hole	0.125 x 0.125	Farnell	5010
1	U1*	IC, Low cost synchronous buck controller	DRC10	TI	TPS40190DRC
1		PCB, 2-Layer FR4, 3.0" x 3.0" x 0.062"	3.0" x 3.0"	Any	TPS40190EVM-001
4		Bumpon, Transparent	0.44" x 0.2"	3M	SJ5303

Table 4: TPS40190EVM-001 Bill of Materials

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